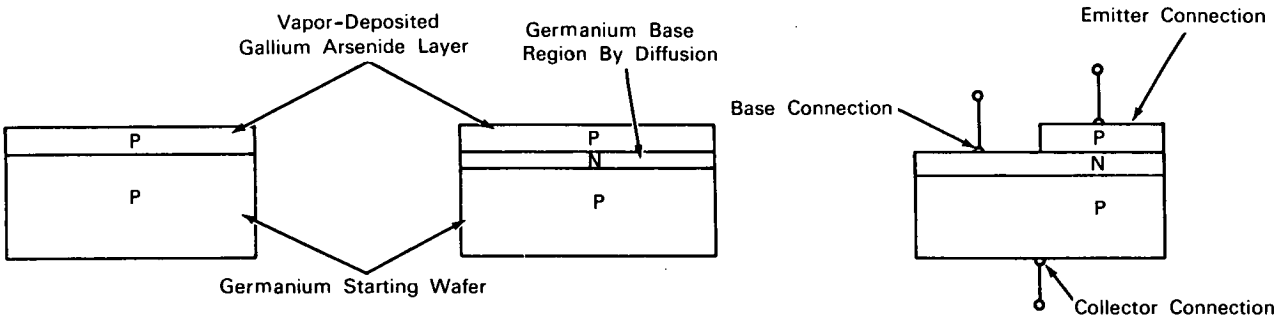
NASA TECH BRIEF

Economical Fabrication Process Produces High-Quality Junction Transistors



The problem: Economical fabrication of a heterojunction-homojunction PNP transistor of high quality.

The solution: A convenient, three-step fabrication process that produces heterojunction-homojunction PNP transistors which exhibit good injection efficiency and low capacitance.

How it's done: A P-type layer of gallium arsenide is vapor-deposited on a P-type starting wafer of germanium. During the growth of the gallium arsenide layer, the vapor pressure and the volatility of the arsenic causes some of it to diffuse into the contiguous region of the starting wafer (center drawing) and form an N-type germanium base region intermediate to the gallium arsenide layer and the germanium starting wafer. The growth period will influence the thickness of the deposited layer and in turn the thickness of the base region.

To facilitate making an ohmic base connection, part of the gallium arsenide layer may be etched away as shown at right. Ohmic emitter and collector connections are made in a conventional manner to the emitter and collector regions.

Notes:

1. Because this transistor has good injection efficiency (low injection loss) and low capacitance, it should improve the performance of communications equipment.
2. Inquiries concerning this innovation may be directed to:

   Technology Utilization Officer
   Jet Propulsion Laboratory
   4800 Oak Grove Drive
   Pasadena, California, 91103
   Reference: B64-10330

Patent status: NASA encourages commercial use of this innovation. No patent action is contemplated.

Source: International Business Machine Corp. under contract to Jet Propulsion Laboratory (JPL-SC-065)

Category No. 01